Title of Investigation:

Miniaturized Imaging Photon Counting Detector System

Principal Investigator:

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Other In-house Members of the Team:

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Initiation Year:

FY 2004

FY 2004 Authorized Funding:

$60,000

Actual or Expected Expenditure of FY 2004 Funding: In-house:

Fabrication, $25,000 (Application Specific Integrated Circuit (ASIC) Dies, $18,000; Printed Wiring Board (PWB), $4,000; ASIC Die Wire bonding, $2,000; Electronics Parts, $1,000); Lab Data-Acquisition (DAQ) Computer and Software Maintenance, $3,500; Lab Equipment Purchase and Repairs, $9,500. Contracts: SWALES (MSES contract for in-house Detector-ASIC PWB Design and Development), $22,000

Status of Investigation at End of FY 2004:

To be continued in FY 2005 with funds remaining from FY 2004 and additional Director's Discretionary Fund (DDF) support in FY 2005 (TBD)

Expected Completion Date:

October 2005

Purpose of Investigation:

The primary purpose of this investigation is to enable new instrument and mission concepts using the Goddard Space Flight Center developed and patented photon-counting laser altimetry and ranging system. Recent instrument studies for applying these techniques to imaging lidars and optical transponders for the upcoming lunar and Mars exploration missions (as well as other solar system exploration missions) have underscored the importance of developing a microelectronics version of the large discrete or hybrid devices we currently have. Imaging lidars provide a three-dimensional map of the target. The target is often the planetary surface, and the resulting data include a digital elevation model and/or information about surface properties, such as tree stand height and density. Optical transponders are capable of providing absolute distance between a station on Earth and a spacecraft to an accuracy of less then 1 cm, with minimal power consumption. Using currently available technology, we would need about 3 watts per timing channel and the designs that most effectively reduce the laser and scanner requirements (and

hence the risk) require approximately 100 pixels or detectors. Consuming 300 or more watts of spacecraft power is not an option; so, we have begun efforts to reduce the power and mass of the lidar receiver's electronics and the receiver's dead time to a few nanoseconds to allow single-shot resolution of vertical structure and roughness.

Specifically, the technology advances needed are the development of: (1) radiation-hardened, compact, low-power, high-event rate and precision-timing electronics; and (2) interfacing techniques to allow the proposed detector, a commercially available multi-anode, micro-channel plate, photo-multiplier tube (MCP-PMT), to be used as an imaging, photon-counting, high-time resolution device. The MCP-PMT was chosen over the current Avalanche Photo-Diode (APD) arrays for its low dead time, short rise time, and high fill factor. The prototype detector system will consist of a 100 anode (pixel) MCP-PMT, high-voltage power converter, harnessing, and Application Specific Integrated Circuit (ASIC) based signal detection and timing circuitry.

Accomplishments to Date:

In an effort to make the most efficient use of the program funds, we negotiated with the Hamamatsu Corporation of Japan to "borrow" a sub-standard engineering-grade detector ($40,000) to evaluate. After considering the issues of interfacing with an 8-GHz signal bandwidth device, it was decided that we needed to solder this device directly to a printed wiring board (PWB) and cut off the excess long anode pins. Hamamatsu agreed to take our partially populated PWB and perform this task with its "loaner" detector and send the PWB back to us.

With regards to the necessary testing of this detector, we secured the use of necessary high-speed test and measurement (T&M) equipment valued at more than $120,000. Using this borrowed equipment, along with our existing ultra-short pulse LED and laser-diode sources, we developed a detector test setup and a refined test procedure using existing representative multi-dynode imaging PMT and single-anode MCP detectors (Figure 1).

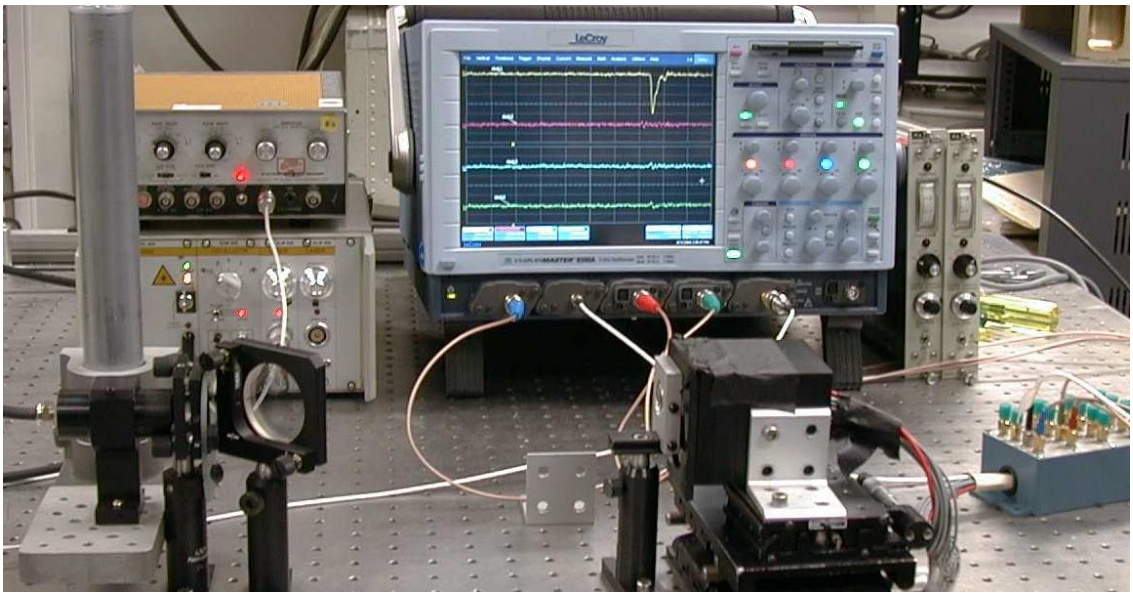

Figure 1. Detector test set-up, with one short-pulsed laser head and a 16-channel PMT

We determined that, for a 16-channel PMT, the dynamic cross-talk between the channels was small enough to be ignored by appropriate choices of discriminator thresholds (Figure 2).

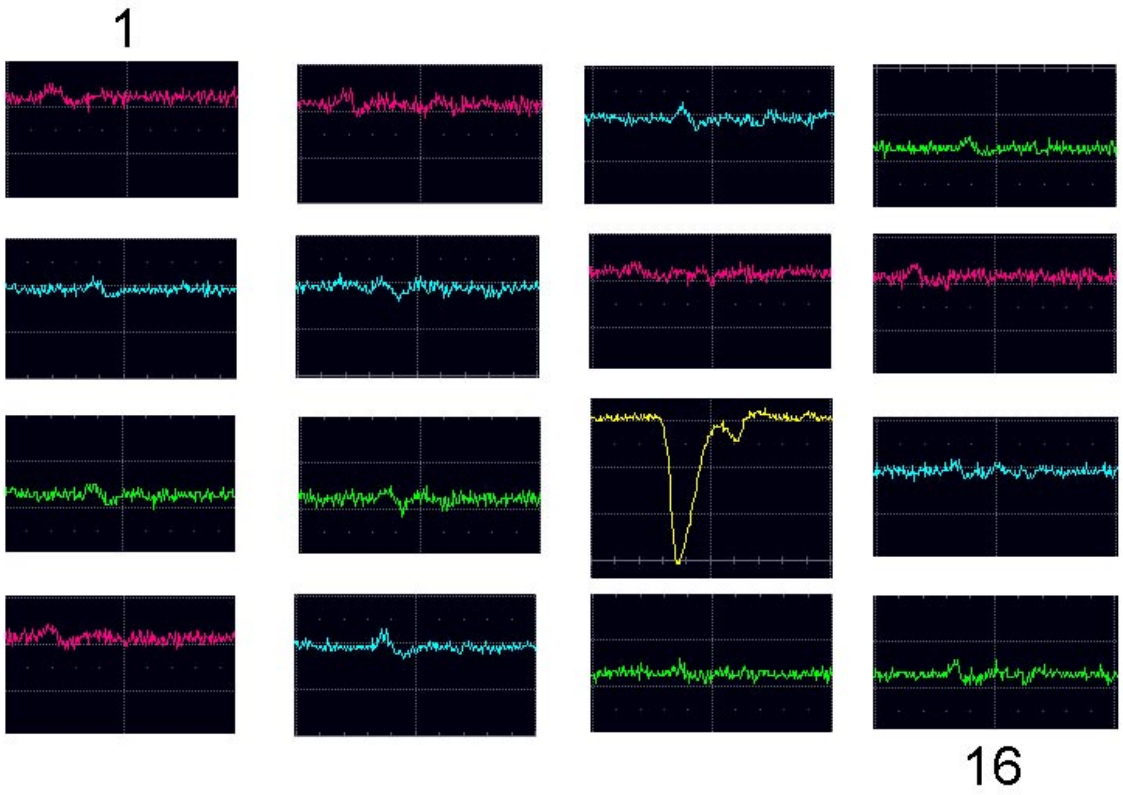

Figure 2. Sixteen-channel PMT cross-talk measurements, with pixel 11 excited and low-induced noise on adjacent pixels

There is still a concern that, due to the higher bandwidth (rise-time) of the MCP signal, longer and closer anode pins, and the sheer number of potentially active channels, we will have to develop a way for the ASIC to discriminate between cross-talk and signal.

After a false start with another support contractor, we have now identified and begun working with the most experience in-house PWB designer for this type of low-noise, high-density, high-speed signal interfacing between the multi-anode MCP and the ASIC dies. After consideration of the 8-10GHz bandwidth and the low energy of the MCP signal, it was decided that we needed to use a chip-on-board approach to keep the wire lengths under 3 cm to minimize the signal distortion due to impedance mismatch.

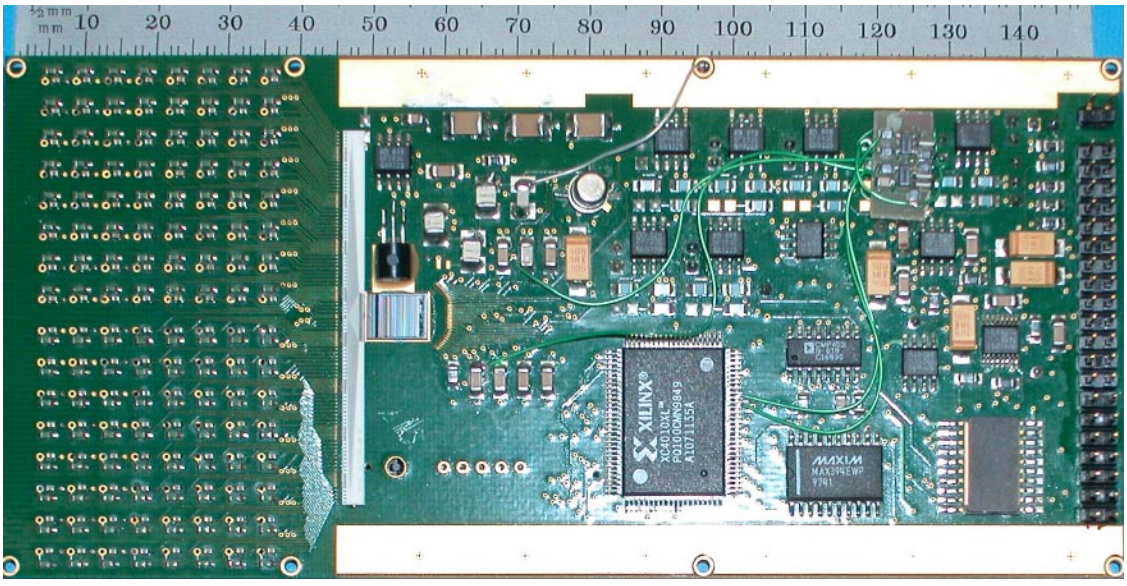

Figure 3. A similar PWB from a previous Goddard Space Flight Center instrument. The detector pins on the left fan down to an ASIC die at the 50-mm position.

To reduce the size and complexity of the ASIC digital input/output to computer harness, it was decided to include a Field Programmable Gate Array (FPGA) to perform the low-level ASIC readout, reconstruction, formatting, and multiplexing of the timing data.

At the start of this effort, we analyzed design concept to determine high-risk device cores to be prototyped on test ASIC 1. Two key core functions were identified as already being prototyped by another mixed-signal timing ASIC development in 564. It was decided that we should wait and incorporate the "lessons-learned" from this other effort and then to share the next ASIC die foundry run to reduce the costs and manpower. This turned out to be fortuitous because errors in the previous design tool library resulted in key circuit traces and features being shorted together on the first Peregrine Semiconductor Silicon on Sapphire (SOS) processed ASIC die (Figure 4), resulting in serious flaws that rendered the part unusable.

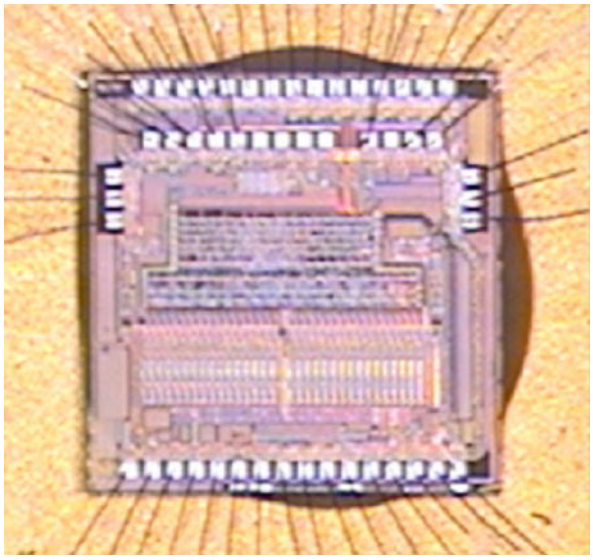

Figure 4. Microscope photo of first Peregrine Semiconductor SOS die

Meanwhile, we designed the basic test cores and laid out the ASIC for the next ASIC foundry run. In both projects, key high-risk core functions will be implemented and tested. An analysis of our design requirements showed that current mode logic was required to achieve the necessary clock speeds and timing resolution. We had to develop the current mode logic library for GHz switching operations in the SOS process for the new and robust manufacturer-supported design tools. We have procured a space in the next multi-project run at the foundry. Figure 5 shows the test ASIC 1 die plots that will be submitted in January.

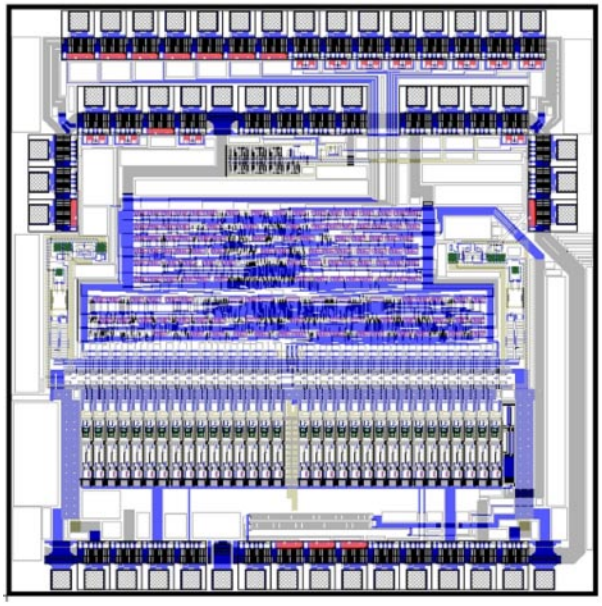

Figure 5. Updated test ASIC 1 die plots

We have now established a complete design-process flow that includes verification of complete design rules and support of the Peregrine Semiconductor SOS process. Unfortunately, this involved determining that the less expensive design tools would not work for this application.

Using our clearer understanding of the technology readiness level (TRL) and what is needed to bring this system to fruition, we submitted three Code T Notices of Intent for instrument development. We also presented a spacecraft tracking and ranging concept and budget for an optical transponder utilizing ASIC technology.

Planned Future Work:

We plan to submit the first test ASIC for fabrication on January 15, 2005, with testing to begin 3 months later. Concurrently, the first fan in/out detector system board will be designed, fabricated,

and partially populated before shipping to Hamamatsu to have a "loaner" detector installed. Testing of the detector and board-level signals will begin upon receipt. The results of the first test ASIC will be used to complete the design of the Prototype Multi-Chan Event Timer (ET) ASIC, which will be submitted for fabrication May 15, 2005. Development of the FPGA-based timer readout logic and interface will begin immediately and be operational when the ET ASIC is delivered on August 15, 2005. After preliminary testing of the ET die, the Integrate Complete 100-pixel detector system will be tested and a final report produced. After successful completion of the IPCDS, it will be integrated in an existing airborne lidar and demonstrated in a relevant application.

Summary:

This project's greatest innovations so far are the custom current mode libraries for the SOS process; the end-to-end ASIC development process; the multi-channel detector test setup; the design concepts to allow testing of the libraries and device performance at >2 GHz clock rates; and the design concepts that will allow reconstruction of absolute epoch time for a random stream of photo-electron events. Successful completion of this effort will advance imaging photon-counting detector technology to a point where Goddard can successfully propose low-laser power, photon-counting imaging Lidar instruments in support of both the Earth and Space Science Enterprises. The system's improved timing resolution and short dead time will allow a new type of scientific measurement to be made using smaller manned and unmanned aircraft and non-low-Earth orbit exploration-sized spacecraft.

Although we have had some successes in key areas of this effort, the primary criterion for success is to duplicate the capability of an entire rack-mounted card crate of electronics in a small handful of integrated circuits that consume less than a hundredth of the power. If we manage to exceed the performance of the existing discrete hardware and match or exceed the 125-psec timing capability of the MCP detector, we will consider this very successful. A secondary success criterion is being able to design a mixed-signal ASIC running at these speeds in the SOS process with confidence that it will work as simulated.

There are risks to being the first to push a new process or technology into new operating regimes or modes. In our case, this resulted in us having to write our own library for operating SOS process-based devices in current mode instead of voltage mode, and also using devices in the existing voltage mode library that had not yet been tested. As a result of the latter, our first test device was unusable and the entire development process was delayed by at least 4 months. There also are risks in developing technologies that have long lead times and infrequent opportunities to re-run a correction. For example, a miscommunication between the foundry supplier and Goddard resulted in an additional 3-month slip in the schedule. While these delays are not showstoppers, they do underscore the importance of doing risky R&D before including such a device in a critical short-development cycle space-flight instrument. In these instances, delays like these dramatically drive up mission costs.